AMENDMENTS TO THE SPECIFICATION

Please replace the last paragraph bridging pages 5 and 6 with the following rewritten paragraph:

[0015]

2, 2a inverter driving unit

3, 3a inverter circuit

4, 4a, 4b, 4c upper arm unit

5, 5a, 5b, 5c lower arm unit

6, 6a bridge circuit

7 DC power supply

8 load

10, 10a high compression IC

12 driver circuit

14 input buffer

16 NMOS transistor

17 parasitic diode

20 resistor

C1, C2, C3, C5 decoupling condenser

D1, D3, D5 upper arm diode

D2, D4, D6 lower arm diode

D10, D11, D12, D13, D21, D22, D23 clamp diode

~~D17 parasitic diode~~

R1, R2, R3, R4, R5, R6 gate resistor

T1, T3, T5 upper arm switching element

T2, T4, T6 lower arm switching element

Please replace the second full paragraph on page 10 with the following rewritten paragraph:

[0027] A mechanism of a malfunction of the high compression IC is described next. In Fig. 2, when the upper arm switching element T1 is turned on, a main circuit current I1 indicated by a dashed line ~~wavy line~~ flows in a load 8 that has an inductance component. When the upper arm switching element T1 is turned off, the current flowing in the load 8 flows through the lower arm diode D2 as a circulating current I2 having an acute inclination and into the load 8. As described above, components in the inverter circuit 3 are connected by patterns and wires, and a slight inductance ~~inducter~~ component is present between the components. Among these inductance components, a position of an inductance component where the circulating current I2 flows is denoted by L11. Assuming that an inductive voltage VL is generated in the inductance component L11 when the circulating current I2 flows through, the inductive voltage VL can be expressed by the following equality.

Please replace the sixth full paragraph on page 11 with the following rewritten paragraph:

[0033] The high compression IC 10 includes the input buffer 14, the NMOS transistor 16, the parasitic diode 17, the resistor 20, and the driver circuit 12, and therefore, when ΔV is applied ~~$\Delta V1$ is applied~~, a through current I3 flows from the parasitic diode 17 through the resistor 20. The through current I3 mainly causes the driver circuit 12 to output an erroneous signal, called the latch up phenomenon.

Please replace the last paragraph bridging pages 11 and 12 with the following rewritten paragraph:

[0034] The inverter device according to the first embodiment includes the clamp diode D10 provided between the lower arm driving reference supply terminal COM and the upper arm driving high-pressure side power supply terminal VB, and therefore, the through current I3 flowing inside the high compression IC 10 in the circuit configuration shown in Fig. 2 can be drawn to the clamp diode D10 side as shown in Fig. 3. Part of the through current might flow in the high compression IC 10, however, an impedance in the clamp diode D10 connected between the same terminal is smaller than an impedance in a series circuit of a parasitic diode 17 ~~diode D17~~ and the resistor 20 through which the through current I3 flows. Therefore, a large portion of the through current I3 can be drawn to the clamp diode D10 side, so that the through current I3 that flows inside the high compression IC 10 can be reduced, and malfunction caused by latch up can be prevented.

Please replace the last paragraph bridging pages 14 and 15 with the following rewritten paragraph:

[0041] The inverter circuit 3a shown in Fig. 4 includes an upper arm unit 4a including the upper arm switching element T1 and the upper arm diode D1 connected back-to-back to each other, an upper arm unit 4b including the upper arm switching element T3 and an upper arm diode D3 connected back-to-back to each other, an upper arm unit 4c including the upper arm switching element T5 and an upper arm diode D5 connected back-to-back to each other, a lower arm unit 5a including the lower arm switching element T2 and a lower arm diode D2 connected back-to-back to each other, a lower arm unit 5b including the lower arm switching element T4 and a lower arm diode D4 connected back-to-back to each other, and a lower arm

unit 5c including the lower arm switching element T6 and a lower arm diode D6 connected back-to-back to each other. Each of the back-to-back connection circuits, the upper arm units 4a, 4b, 4c, are connected in series to each of the back-to-back connection circuits, the lower arm units 5a, 5b, 5c ~~the lower arm units 5a~~, respectively, in a bridge circuit 6a. In the bridge circuit 6a, the positive electrode of the DC power supply 7 is connected to each corrector of the upper arm switching elements T1, T3, T5, and the negative electrode of the DC power supply 7 is connected to each emitter of the lower arm switching elements T2, T4, T6. Thus, the inverter circuit 3a shown in Fig. 4 has a configuration of a three-phase inverter circuit.

Please replace the last paragraph bridging pages 15 and 16 with the following rewritten paragraph:

[0044] In between the inverter circuit 3a and the high compression IC 10a, each terminal of the upper arm switching element driving signal output terminals HO1, HO3, HO5 and each gate of the upper arm switching elements T1, T3, T5 are connected by gate resistors R1, R3, R5, respectively. Each terminal of the upper arm driving reference supply terminals VS1, VS3, VS5 is directly connected to each emitter of the upper arm switching elements T1, T3, T5 ~~upper arm switching elements T1~~, respectively. Similarly, each terminal of the lower arm switching element driving signal output terminals LO2, HO4, HO6 ~~LO1, HO3, HO5~~ and each gate of the lower arm switching elements T2, T4, T6 are connected by gate resistors R2, R4, R6, respectively. The lower arm driving reference supply terminal COM is directly connected to each emitter of the lower arm switching elements T2, T4, T6 ~~lower arm switching elements T2~~.

Please replace the second full paragraph on page 16 with the following rewritten paragraph:

[0046] Thus, in the inverter device according to the second embodiment, similarly to the first embodiment, a large portion of through current flowing toward the inside of the high compression IC 10a can be drawn to the side of the clamp diodes D11, D12, D13, so that the through current that flows toward the high compression IC 10a ~~high compression IC 10~~ can be reduced, and malfunction caused by latch up can be prevented.

Please replace the first full paragraph on page 19 with the following rewritten paragraph:

[0053] Thus, in the inverter device according to the third embodiment, similarly to the inverter devices according to the first and second embodiments, a large portion of through current flowing toward the inside of the high compression IC 10a can be drawn to the side of the first clamp diode D10 and the second clamp diodes D21, D22, D23 ~~D11, D12, D13~~, so that the through current that flows toward the inside the high compression IC 10a ~~high compression IC 10~~ can be reduced, and malfunction caused by latch up can be prevented.